	Type	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition
1	BRS	22	simultaneous with bidirectional with port with circuit$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/27 13:45		
2	BRS	0	simultaneous with bidirectional with port with circuit$1 and sampl$3 with waveform and (storage or memory) and (processor$1 or microprocessor$1 or controller$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/27 13:47		
3	BRS	2	simultaneous with bidirectional with port with circuit$1 and waveform$1 and (storage or memory) and (processor$1 or microprocessor$1 or controller$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/27 13:51		
4	BRS	0	on-die adj waveform$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/27 13:48		
5	BRS	5	on-die with waveform$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/27 13:49		

	Type	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition
6	BRS	125	(bi-directional or bidirectional) with port$1 with circuit$1 and waveform$1 and (storage or memory) and (processor$1 or microprocessor$1 or controller$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/27 13:51		
7	BRS	83	(bi-directional or bidirectional) with port$1 with circuit$1 and waveform$1 and (storage or memory) and (processor$1 or microprocessor$1 or controller$1) and receiver$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/27 14:53		
8	BRS	1	(bi-directional or bidirectional) with port$1 with circuit$1 and waveform$1 and (storage or memory) and (processor$1 or microprocessor$1 or controller$1) and receiver$1 with offset with comparator$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/27 15:53		

	Type	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition
9	BRS	25	(bi-directional or bidirectional) with port$1 with circuit$1 and waveform$1 and (storage or memory) and (processor$1 or microprocessor$1 or controller$1) and receiver$1 with (threshold$1 or predetermin$3 or reference$1 or expected or desired or predefin$2)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/28 13:37		
10	BRS	16	(bi-directional or bidirectional) with port$1 with circuit$1 and waveform$1 and (storage or memory) and (processor$1 or microprocessor$1 or controller$1) and receiver$1 with (threshold$1 or predetermin$3 or reference$1 or expected or desired or predefin$2) and time with point$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/27 14:52		

	Type	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition
11	BRS	0	(bi-directional or bidirectional) with port$1 with circuit$1 with time with point$1 and waveform$1 and (storage or memory) and (processor$1 or microprocessor$1 or controller$1) and receiver$1 with (threshold$1 or predetermin$3 or reference$1 or expected or desired or predefin$2)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/27 14:01		
12	BRS	0	sampl$3 with (bi-directional or bidirectional) with port$1 with circuit$1 with time with point$1 and receiver$1 with receiv$3 and (vary$3 or calibrat$3 or chang$3 or adjust$3 or modify$3) with (threshold$1 or predetermin$3 or reference$1 or expected or desired or predefin$2)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/27 14:07		
13	BRS	0	6621323.uref.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/27 14:42		

	Type	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition
14	BRS	1	"6496058".PN.	USPAT	2004/10/27 14:39		
15	BRS	1	"6127849".PN.	USPAT	2004/10/27 14:40		
16	BRS	1	"5793223".PN.	USPAT	2004/10/27 14:40		
17	BRS	207	702/122.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/27 14:43		
18	BRS	5580	326/21,26,27,28,30,31,35,82,83,86.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/27 14:44		
19	BRS	3292	327/108,109,110,379,386,387.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/27 16:17		

	Type	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition
20	BRS	1	(bi-directional or bidirectional) with port$1 with circuit$1 and waveform$1 and (storage or memory) and (processor$1 or microprocessor$1 or controller$1) and receiver$1 with (threshold$1 or predetermin$3 or reference$1 or expected or desired or predefin$2) and time with point$1 and shift with register	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/27 14:52		
21	BRS	6	(bi-directional or bidirectional) with port$1 with circuit$1 and waveform$1 and (storage or memory) and (processor$1 or microprocessor$1 or controller$1) and receiver$1 with (threshold$1 or predetermin$3 or reference$1 or expected or desired or predefin$2) and time with point$1 and shift	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/27 14:52		

	Type	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition
22	BRS	23	(bi-directional or bidirectional) with port$1 with circuit$1 and waveform$1 and (storage or memory) and (processor$1 or microprocessor$1 or controller$1) and receiver$1 and shift$3 with register	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/27 14:54		
23	BRS	67	(bi-directional or bidirectional) with port$1 with circuit$1 and waveform$1 and (storage or memory) and (processor$1 or microprocessor$1 or controller$1) and receiver$1 and driver$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/27 14:54		
24	BRS	4	(326/$.ccls. or 327/$.ccls.) and (bi-directional or bidirectional) with port$1 with circuit$1 and waveform$1 and (storage or memory) and (processor$1 or microprocessor$1 or controller$1) and receiver$1 and driver$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/27 14:57		

	Type	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition
25	BRS	42	(bi-directional or bidirectional) with port$1 with circuit$1 and waveform$1 and (storage or memory) and (processor$1 or microprocessor$1 or controller$1) and receiver$1 and driver$1 and count$3	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/27 14:57		
26	BRS	37	(bi-directional or bidirectional) with port$1 with circuit$1 and waveform$1 and (storage or memory) and (processor$1 or microprocessor$1 or controller$1) and receiver$1 and driver$1 and counter	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/27 14:57		
27	BRS	19	(bi-directional or bidirectional) with port$1 with circuit$1 and waveform$1 and (storage or memory) and (processor$1 or microprocessor$1 or controller$1) and receiver$1 and driver$1 and counter and shift$3 with register	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/27 15:00		

	Type	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition
28	BRS	30	(bi-directional or bidirectional) with port$1 with circuit$1 and waveform$1 and (storage or memory) and (processor$1 or microprocessor$1 or controller$1) and receiver$1 and driver$1 and counter and comparator$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/27 15:02		
29	BRS	0	326/35.ccls. and (bi-directional or bidirectional) with port$1 with circuit$1 and waveform$1 and (storage or memory) and (processor$1 or microprocessor$1 or controller$1) and receiver$1 and driver$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/27 15:02		
30	BRS	47	(bi-directional or bidirectional) with port$1 with circuit$1 and waveform$1 and (storage or memory) and (processor$1 or microprocessor$1 or controller$1) and receiver$1 and network	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/27 15:54		

	Type	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition
31	BRS	28	(bi-directional or bidirectional) with port$1 with circuit$1 and waveform$1 and (storage or memory) and (processor$1 or microprocessor$1 or controller$1) and receiver$1 and network with interface	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/27 15:54		
32	BRS	0	(bi-directional or bidirectional) with port$1 with circuit$1 with nose and waveform$1 and (storage or memory) and (processor$1 or microprocessor$1 or controller$1) and receiver$1 and network with interface	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/27 15:55		
33	BRS	0	(bi-directional or bidirectional) with port$1 with circuit$1 with nose and waveform$1 and (storage or memory) and (processor$1 or microprocessor$1 or controller$1) and receiver$1 and network with (communication or interface)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/27 15:55		

	Type	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition
34	BRS	0	(bi-directional or bidirectional) with port$1 with circuit$1 with nose and waveform$1 and receiver$1 and network with (communication or interface)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/27 15:55		
35	BRS	0	(bi-directional or bidirectional) with port$1 with circuit$1 with node and waveform$1 and (storage or memory) and (processor$1 or microprocessor$1 or controller$1) and receiver$1 and network with interface	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/27 15:56		
36	BRS	0	(bi-directional or bidirectional) with port$1 with circuit$1 with node and waveform$1 and receiver$1 and network with interface	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/27 16:09		
37	BRS	0	(bi-directional or bidirectional) with port$1 with circuit$1 with node with network and waveform$1 and receiver$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/27 16:10		

	Type	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition
38	BRS	1	(bi-directional or bidirectional) with port$1 with circuit$1 with node and network and waveform$1 and receiver$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/27 16:10		
39	BRS	1	(bi-directional or bidirectional) with port$1 with circuit$1 with node and network and waveform$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/27 16:11		
40	BRS	2	(bi-directional or bidirectional) with port$1 with circuit$1 with waveform$1 and network	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/27 16:11		
41	BRS	84	(bi-directional or bidirectional) with port$1 with circuit$1 and network and waveform$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/27 16:12		
42	BRS	21	(bi-directional or bidirectional) with port$1 with circuit$1 with network and waveform$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/27 16:14		
43	BRS	15	(bi-directional or bidirectional) with port$1 with circuit$1 with network and receiv$3 with digital with data	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/27 16:21		

	Type	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition
44	BRS	0	(327/108,109,110,379,386,387.ccls.) and (bi-directional or bidirectional) with port$1 with circuit$1 with network and receiv$3 with digital with data	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/27 16:18		
45	BRS	1	(327/108,109,110,379,386,387.ccls. or 326/21,26,27,28,30,31,35,82,83,86.ccls.) and (bi-directional or bidirectional) with port$1 with circuit$1 with network and receiv$3 with digital with data	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/27 16:18		
46	BRS	1	(bi-directional or bidirectional) with integrated with circuit and port$1 with circuit$1 with network and receiv$3 with digital with data	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/27 16:22		
47	BRS	2	(bi-directional or bidirectional) with integrated with circuit and port$1 with circuit$1 with network and receiv$3 with driver$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/27 16:22		

	Type	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition
48	BRS	0	electronic and integrated with circuit$1 and (bi-direction$2 or bidirection$2) and port with circuit41 and node$1 with receiv$3 and network with interface	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/28 13:34		
49	BRS	1	"6496058".PN.	USPAT	2004/10/28 13:28		
50	BRS	1	"6127849".PN.	USPAT	2004/10/28 13:29		
51	BRS	117	electronic and integrated with circuit$1 and (bi-direction$2 or bidirection$2) and port with circuit$1 and node$1 with receiv$3 and network with interface	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/28 13:35		
52	BRS	253	electronic and integrated with circuit$1 and (bi-direction$2 or bidirection$2) and port with circuit$1 and node$1 with receiv$3	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/28 13:35		
53	BRS	11	electronic and integrated with circuit$1 and (bi-direction$2 or bidirection$2) and port with circuit$1 and node$1 with receiv$3 and network with interface and waveform	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/28 13:36		

	Type	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition
54	BRS	83	(bi-directional or bidirectional) with port$1 with circuit$1 and waveform$1 and (storage or memory) and (processor$1 or microprocessor$1 or controller$1) and receiver$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/28 13:41		
55	BRS	2	(bi-directional or bidirectional) and port$1 with circuit$1 with waveform$1 and (storage or memory) and (processor$1 or microprocessor$1 or controller$1) and receiv$3 with node$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/28 13:38		
56	BRS	52	(bi-directional or bidirectional) with port$1 with circuit$1 and waveform$1 and (storage or memory) and (processor$1 or microprocessor$1 or controller$1) and receiver$1 and integrated with circuit$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/28 13:41		